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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,333	02/09/2004	Hiroshi Okumura	Q77321	8920

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,333	OKUMURA, HIROSHI	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *18-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13,14 and 16* is/are rejected.

7)☒ Claim(s) *12,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response filed 6/9/05 forms the basis of this office action. Claims 18-28 have been cancelled. Comments on Remarks in said Response are provided below under "Response to Arguments".

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement (IDS) filed 6/9/05 but only to the extent possible: examiner does not read Japanese. Therefore, only the English abstract of all items 1-4 in said IDS have been considered. A signed copy of the Form PTO-1449 is herewith enclosed.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show gate electrode 107 as the two-layer film as described in the specification (see page 9, [29]). Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement

sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1-3 and 4-6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view of Lee et al (6,124,153) and Yanai et al (US 2003/0025127 A1). Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304) formed above said insulating substrate (cf. Figure 1), wherein said first thin film transistor comprises a first active layer 302 (island-like portion to the left in Figure 1; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active

layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode formed 307 (see [03]) on said second gate insulating film,

wherein a thickness of said second gate insulating film 303/306 is larger than a thickness of said first gate insulating film 303, by the thickness of 306 (see [03]),

wherein said second active layer 302 has at least two impurity doping regions 305b (see [03]) which overlap said second gate electrode 307,

wherein said second gate electrode comprises a semiconductor layer (polysilicon layer; see [02]).

Prior Art as Admitted by Applicant also teaches said first active layer has at least two impurity doping regions 305a, but does not necessarily teach the limitation that said at least two impurity doping regions are formed in a self-aligning manner with respect to said first gate electrode. *However, it would have been obvious to include said limitation in view of Yanai et al,* who teach for the specific purpose (see [0040]) of simplifying the manufacturing process in a semiconductor TFT device comprising both a low-voltage driven TFT region and a high-voltage driven TFT region, the impurity regions of the low-

voltage driven TFT can be formed in self-alignment (see abstract, and [0040], [0148]-[0150], Figure 4A).

Furthermore, although met by Yanai et al as discussed above, the limitation "formed in a self-aligning manner with respect to said gate electrode" only has patentable weight in the result for the final structure. In reference to the claim language referring to "formed in a self-aligning manner with respect to said gate electrode" intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).*

Finally, neither Prior Art admitted by Applicant nor Yanai et al necessarily teach the limitation that said second gate electrode comprises a semiconductor layer. However, it would have been obvious to include said limitation in view of Lee et al, who, in a patent on a polysilicon TFT (see title), hence closely related to Prior Art as admitted by Applicant, teach the selection of polysilicon as a preferable material for the gate electrode in a TFT (col. 2, l. 58-62). *Motivation* to include the teaching by Lee et al derives from (a) the electrically conductive nature of the polysilicon used (col. 3, l. 57-61) and (b) polysilicon is already used for the active region of the Prior Art as admitted by Applicant ([02]) and hence the selection of polysilicon also for the gate electrode does not complicate the process of manufacture. Applicant is also reminded that it has been held that mere selection of known materials generally understood to be suitable to

make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

On claim 2: said second gate insulating film comprises said first gate insulating film 303 and a gate cover film 306 above said first gate insulating film (see [03]).

On claim 3: the limitation as defined by claim 3 is not necessarily taught by either the Prior Art as Admitted by Applicant, nor by Yanai et al. However, Yanai et al do teach said at least two impurity doping regions of the first active layer to be formed by self-aligning with a thickness of the first gate insulating film that is 30 nm (see Abstract), - which is a fraction of the claimed overlap of 100 nm (=0.1 μm), in this context teaching that the LDD region portion 120 ([0152], [0160]) of one of said at least two impurity doping regions in one of two low-voltage TFTs (namely, the n-type TFT in a CMOS driver (consisting of a n-type TFT and a p-type TFT) (i.e., low in comparison to a pixel TFT; see Abstract, final sentence)) is located "just below" a drain-side edge of the gate electrode (see [0152]). Any overlap is thus seen to be of the order of or less than 30 nm. Applicant, in the Specification, does not explain why the difference between the gate-drain overlap between the gate and an LDD region formed by self-alignment just below a 30 nm thick gate insulating film and the claimed overlap 100nm or less is critical to his invention. Applicant's disclosure does not teach why the difference between the range implicit in the prior art as cited here and the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are

disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller, 105 USPQ 233.*

On claim 4: at least one of said impurity doping regions formed in a self-aligning manner with respect to said first gate electrode includes an LDD structure 120 ([0152] and [0160]).

On claim 6: at least one of said impurity doping regions which overlap said second gate electrode includes an LDD structure (Abstract, final sentence).

3. ***Claim 5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Lee et al and Yanai et al as applied to claim 1 above, and further in view of Oh (5,610,082). *As detailed above, claim 1 is unpatentable* over Prior Art as Admitted by Applicant in view of Lee et al and Yanai et al. *Neither Prior Art admitted by Applicant nor Lee et al nor Yanai et al necessarily teach* the further limitation as defined by claim 5. *However, it would have been obvious* to include said further limitation in view of Oh, who teach a gate-drain overlap of a switching TFT (Figure 3 and Background of the Invention, particularly col. 3, l. 8-27) that it is preferable to have a gate-drain overlap of between 1 – 2 μm. *Motivation* to include the teaching by Oh in the invention by the Prior Art as Admitted by Applicant is the consideration by Oh that parasitic capacitance limits the desirable overlap to below 2 μm (loc.cit.). Furthermore, Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close

enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

4. ***Claims 7-8*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Lee et al and Yanai et al as applied to claim 1 above, and further in view of Okumura (JP 11307777 A) (IDS). *As detailed above, claim 1 is unpatentable over the Prior Art as Admitted by Applicant in view of Lee et al and Yanai et al. Neither Prior Art as Admitted by Applicant nor Lee et al nor Yanai et al necessarily teach* the further limitation as defined by claim 7. *However, it would have been obvious to include said further limitation in view of Okumura*, who in a patent document on TFTs for liquid crystal displays, hence closely related art and a/o including both low- and high-voltage transistors (namely: driver transistors (claim 7) and pixel transistors (claim 8), respectively), teaches the gate electrode to comprise a semiconductor layer 5 and a metal layer 6 (cf. Abstract) for the purpose of achieving high reliability and low cost (cf. Abstract). *Motivation* to include the teaching by Okumura in the invention at least derives from the stated high reliability and the lower resistance in comparison to a single polysilicon gate as taught by the Prior Art as Admitted by Applicant. *Combination* is easily achieved by adding to the polysilicon gate a metal film.

5. ***Claims 9 and 10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicant, Lee et al and Yanai as applied to claims 1 and 2, respectively, above, and further in view of Nakamura (JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05). As detailed above, claims 1 and 2 are unpatentable over Prior Art admitted by Applicant in view of Lee et al and Yanai, none

necessarily teaching the further limitations of claims 9 or 10. However, it would have been obvious to include said further limitations in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode 13 between an active layer and a gate electrode 17 with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

6. ***Claims 11 and 16*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view of Yanai and Nakamura (JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05). Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304) formed above said insulating substrate (cf. Figure 1), wherein said first thin film transistor comprises a first active layer 302 (island-like portion to the left in Figure 1; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode formed 307 (see [03]) on said second gate insulating film,

wherein a thickness of said second gate insulating film 303/306 is larger than a thickness of said first gate insulating film 303, by the thickness of 306 (see [03]),

wherein said second active layer 302 has at least two impurity doping regions 305b (see [03]) which overlap said second gate electrode 307.

Prior Art as admitted by Applicant does not necessarily teach the further limitations (a) "wherein said first active layer has at least two impurity doping regions formed in a self-aligning manner with respect to said first gate electrode" and (b) "wherein said second thin film transistor further comprises a third gate electrode formed between said second active layer and said second gate electrode.

However, it would have been obvious to include further limitation ad (a) in view of Yanai who teaches (see [0029]) that for low-voltage transistors self-aligned source/drain regions are preferable because (1) overlap is not needed because of the absence of the hot-electron problem (hot electrons actually are highly accelerated electrons) and (2) self-alignment improves the accuracy and enables making very small devices (see [0029]). *Motivation* to include the teaching by Yanai in this regard is the advantage of higher device density through self-alignment without the danger of hot-electron effects

because the transistor with gate 304 in the Prior Art as admitted by Applicant is also a low-voltage device.

Furthermore, it would have been obvious to include the further limitation ad (b) in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode 13 between an active layer and a gate electrode 17 with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

On claim 16: at least one of said impurity doping regions that overlap said second gate electrode includes an LDD structure 14 (see English abstract in Nakamura), which would have been obvious to include in the prior art as admitted by Applicant because LDD regions counteract hot electron effects. Motivation to include the teaching on LDD structure by Nakamura is the avoidance of hot electron effects in the high-voltage transistor.

7. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicant, Yanai and Nakamura as applied to claim 11 above, and further in view of Adler et al (5,757,050). As detailed above, claim 11 is unpatentable over Prior Art as admitted by Applicant, in view of Yanai and Nakamura, none necessarily teaching the further limitation defined by claim 13. However, it would have been obvious to include said further limitation in view of Adler et al who teach a thin film transistor that is self-aligned (col. 2, l. 50-59) and with overlap by 0.1 mm or less (col. 8,

l. 24-43). Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

8. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as admitted by Applicant, Yanai and Nakamura as applied to claim 11 above, and further in view of Zhang et al (6,507,069 B1). As detailed above, claim 11 is unpatentable over Prior Art as admitted by Applicant in view of Yanai and Nakamura, none however necessarily teaching the further limitation defined by claim 14. However, it would have been obvious to include said further limitation in view of Zhang et al, who, in a patent on thin film transistors, hence analogous art, teach self-aligned thin film transistors to include LDD regions for the specific reason to reduce the OFF current (col. 2, l. 9-15). *Motivation* to include the teaching by Zhang thus derives from the obvious advantage to reduce the inherently unwanted current in the OFF state.

Allowable Subject Matter

9. ***Claims 12, 15 and 17*** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: within the context of the invention as defined by claim 11 the third gate electrode's thickness (claim 12) and two-layer

structure (claim 15 nor the overlap range for the second electrode as recited in claim 15 are found in the prior art.

Response to Arguments

10. Applicant's arguments, see Response filed 6/9/05, with respect to the rejections of claims 1-8 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Lee et al (6,124,153). Accordingly, previous rejections have been supplemented by including Lee et al to teach explicitly a gate electrode of polysilicon. Additionally,

(a) an objection to the drawings is included as it is noted that gate electrode 107 is disclosed to be a two-layer film but the Drawings do not show said gate electrode as a two-layer film; while

(b) the IDS has prompted reconsideration of the indication of allowable subject matter, judging from the English abstract of Nakamura JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05) for claims 9, 10, 11, 13 and 16.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Okumura (JP 11307777 A) (made of record by Applicant through IDS filed 6/9/05) also teach gate electrode of polysilicon, judging from the English abstract.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
August 17, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 2826)